



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/805,113

03/19/2004

Neil G. Jacobson

X-1550 US

8497

24309

7590

11/12/2008

XILINX, INC

ATTN: LEGAL DEPARTMENT

2100 LOGIC DR

SAN JOSE, CA 95124

EXAMINER

ABAD, FARLEY J

ART UNIT

PAPER NUMBER

2181

MAIL DATE

DELIVERY MODE

11/12/2008

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/805,113	<b>Applicant(s)</b> JACOBSON ET AL.	
	<b>Examiner</b> FARLEY J. ABAD	<b>Art Unit</b> 2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 12 August 2008.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>12 August 2008</u> .  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### **Status of claims:**

1. Claims 1-20 are pending in the present application.
2. Claims 1-6, 11, 15, 16, 17, 19, and 20 are amended.
3. Claims 8 and 10 are cancelled.

### ***Response to Arguments***

4. Applicant's arguments with respect to claims 1-7 and 11-20 have been considered but are moot in view of the new ground(s) of rejection.

### ***Information Disclosure Statement***

5. The information disclosure statement (IDS) submitted on 08/12/2008 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

### ***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. **Claims 1, 2, 4, 5, 9, 15, 17, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lulla et al (hereinafter Lulla), U.S. Patent No. 6,922,820 B1, in view of Geer et al (hereinafter Geer), U.S. Patent No. 5,079,725, and in further view of Aralis et al (hereinafter Aralis), U.S. Patent No. 5,319,598.**

**As per claim 1**, Lulla discloses a method for identifying and configuring a system, comprising:

reading values of identification codes [fig. 3, elements 102-108, col. 3, lines 48-50, col. 3, lines 1-12, identification codes 102-108 are read to generate an IDCD] from each of a first plurality of devices of a first system [col. 2, lines 64-67, col. 3, line 1, 15-16, 36-50, portions 102-108 are equivalent to a plurality of devices since each portion of the register 100 may be comprised of separate bits];

generating a first system identifier value that identifies the first system as a function of the read values [col. 3, lines 44-48, the IDCD code is generated which identifies the system 90 as a function of the identification codes 102-108].

Lulla does not explicitly disclose wherein the first plurality of devices is arranged and coupled in a scan chain, and the function used in generating the first system identifier value is further a function of respective positions of the first plurality of devices in a scan chain.

However, Geer discloses the use of wherein the first plurality of devices is arranged and coupled in a scan chain, and the function used in generating the first system identifier value is further a function of respective positions of the first plurality of devices in a scan chain [col. 5, lines 29-35, the plurality of SRLs are arranged and

Art Unit: 2181

coupled in a scan chain (fig. 1, SRLs 14 and 16). Retrieving the identification number is equivalent to generating the system identifier. The function of retrieving the identification number is a function of the locations of the SRLs in the scan chain, specifically “the chip ID or level ID SRLs indicating the location of the SRLs to retrieve the stored identification number.” The location of the SRLs is equivalent to the positions of the plurality of devices in a scan chain].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve upon the method of Lulla by implementing wherein the first plurality of devices is arranged and coupled in a scan chain, and the function used in generating the first system identifier value is further a function of respective positions of the first plurality of devices in a scan chain because it would provide Lulla’s method with the enhanced capability of uniquely identifying integrated circuit chips adapted for use with scan design system and scan testing techniques [p. 2, paragraph 19-23].

The modified Lulla does not explicitly disclose storing the first system identifier value in association with respective configuration data sets for the first plurality of devices;

reading values of identification codes from each of a second plurality of devices coupled in a scan chain in a target system;

generating a target system identifier value that identifies the target system as a function of the values read from the second plurality of devices and respective positions of the second plurality of devices in the scan chain;

comparing the stored first system identifier value to the target system identifier value;

configuring the second plurality of devices in the target system with the respective configuration data sets in response to the stored first system identifier value matching the target system identifier value; and

halting configuring of the second plurality of devices in the target system in response to the stored first system identifier value not matching the target system identifier value.

However, Aralis discloses storing the first system identifier value [figs. 1 and 4, ID code stored in memory 34] in association with respective configuration data sets [figs. 1 and 4, col. 4, lines 38-43, configuration data is stored in shift register 36] for the first plurality of devices [fig. 4, devices 200-204];

reading values of identification codes from each of a second plurality of devices [figs. 1 and 4, col. 3, lines 60-68, col. 4, lines 12-21, col. 7, lines 49-55, ID codes for each device 34 can be read from SDO 54 by pulsing READ 48 high] coupled in a scan chain in a target system [fig. 4];

generating a target system identifier value [col. 4, lines 26-32, after reading each device's ID code a serial bit stream is generated, which is equivalent to a target system identifier value since the bit stream will contain the ID codes of all the devices to be configured] that identifies the target system as a function of the values read from the second plurality of devices and respective positions of the second plurality of devices in

Art Unit: 2181

the scan chain [col. 7, lines 55-58, the serial bit stream will contain the IDs of all devices in order];

comparing the stored first system identifier value to the target system identifier value [col. 4, lines 38-45, ID code in memory 34 is compared to the interrogation code (serial bit stream shifted into register 38)];

configuring the second plurality of devices in the target system with the respective configuration data sets in response to the stored first system identifier value matching the target system identifier value [col. 4, lines 45-55]; and

halting configuring of the second plurality of devices in the target system in response to the stored first system identifier value not matching the target system identifier value [col. 8, lines 58-60, programming is inhibited by an incorrect match of codes] for the purpose of providing configurable circuits which may be difficult to access [col. 1, lines 42-50].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve upon the modified Lulla by implementing storing the first system identifier value in association with respective configuration data sets for the first plurality of devices;

reading values of identification codes from each of a second plurality of devices coupled in a scan chain in a target system;

generating a target system identifier value that identifies the target system as a function of the values read from the second plurality of devices and respective positions of the second plurality of devices in the scan chain;

comparing the stored first system identifier value to the target system identifier value;

configuring the second plurality of devices in the target system with the respective configuration data sets in response to the stored first system identifier value matching the target system identifier value; and

halting configuring of the second plurality of devices in the target system in response to the stored first system identifier value not matching the target system identifier value because it would provide the modified Lulla with the enhanced capability of providing configurable circuits which may be difficult to access [col. 1, lines 42-50].

**As per claim 2**, Lulla discloses the method of claim 1, wherein the step of reading values from the first plurality of devices comprises:

reading the value of a first register in each of the first plurality of the devices [fig. 3, register 100 is in the devices 102-108], wherein the state of each first register is a non-programmable value [col. 1, lines 57-58].

**As per claim 4**, Lulla discloses the method of claim 1, wherein the step of reading values from the first plurality of devices comprises:

inputting a control code to each of the first plurality of devices  
outputting the values of the identification codes serially from at least one of the first plurality of devices in response to the control code [fig. 4, col. 3, lines 36-50].

**As per claim 5**, Lulla discloses the method of claim 1, wherein the step of reading values from the first plurality of devices further comprises:



reading values from registers in the first plurality of devices, wherein each register is user-programmable [col. 4, lines 54-58, specifically user software VERILOG, used to provide device ID's].

**As per claim 9**, Lulla discloses the method of claim 1, wherein the generating step includes concatenating the values [col. 5, line 6].

**As per claim 15**, Lulla discloses the method of claim 1, wherein the first plurality of devices are programmable logic devices [col. 1, lines 6-9] and the values of identification codes from each of the first plurality of programmable logic devices is a configuration state of the programmable logic device [col. 3, lines 51-63, specifically CNFG and DEV indicate a state of the device. CNFG and DEV are inputs to the ID CODE GENERATION LOGIC which outputs the identification code, fig. 4].

**As per claim 17**, Lulla discloses the method of claim 1, wherein the system includes a plurality of non-volatile memories coupled to the first plurality of devices [col. 2, lines 54-59], the devices are boundary-scan accessible [col. 2, lines 64-66], and the reading of values from the first plurality of devices includes reading the values of the identification codes from the plurality of non-volatile memories [col. 2, lines 54-59].

**As per claim 19**, Lulla discloses an apparatus for identifying and configuring a system, comprising:

means for [fig. 3, TDO 94] reading values of identification codes [fig. 3, elements 102-108, col. 3, lines 48-50, col. 3, lines 1-12, identification codes 102-108 are read to generate an IDCD] from a first plurality of devices of a first system [col. 2, lines 64-67,

Art Unit: 2181

col. 3, line1, lines 15-16, portions 102-108 are equivalent to a plurality of devices of the system since each portion can have separate bits];

means for [col. 2, lines 45-46, JTAG identification request] generating a first system identifier value as a function of the values of the identifications codes from the first plurality of devices [col. 3, lines 44-48, the IDCD code is generated which identifies the system 90 as a function of the identification codes 102-108].

Lulla does not explicitly disclose wherein the first plurality of devices is arranged and coupled in a scan chain, and the function used in generating the first system identifier value is further a function of respective positions of the first plurality of devices in a scan chain.

However, Geer discloses the use of wherein the first plurality of devices arranged and coupled in a scan chain, and the function used in generating the first system identifier value is further a function of respective positions of the first plurality of devices in a scan chain [col. 5, lines 29-35, the plurality of SRLs are arranged and coupled in a scan chain (fig. 1, SRLs 14 and 16). Retrieving the identification number is equivalent to generating the system identifier. The function of retrieving the identification number is a function of the locations of the SRLs in the scan chain, specifically “the chip ID or level ID SRLs indicating the location of the SRLs to retrieve the stored identification number.” The location of the SRLs is equivalent to the positions of the plurality of devices in a scan chain].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve upon the method of Lulla by implementing wherein the

Art Unit: 2181

first plurality of devices arranged and coupled in a scan chain, and the function used in generating the first system identifier value is further a function of respective positions of the first plurality of devices in a scan chain because it would provide Lulla's apparatus with the enhanced capability of uniquely identifying integrated circuit chips adapted for use with scan design system and scan testing techniques [p. 2, paragraph 19-23].

Furthermore, taking claim 1 as exemplary, claim 19 is directed to similar limitations as claim 1 [see claim 1]. Therefore, claim 19 is rejected under the same rationale as claim 1, and in further view of Aralis.

**As per claim 20**, Lulla discloses an arrangement for identifying and configuring a system, comprising:

a software tool hosted on a data processing arrangement [fig. 4]; and

a system interface coupled to the tool and to a first system [fig. 3];

wherein the tool is configured to read values of identification codes [fig. 3, elements 102-108, col. 3, lines 48-50, col. 3, lines 1-12, identification codes 102-108 are read to generate an IDCD] from each of a first plurality of devices of the system [col. 2, lines 64-67, col. 3, line1, lines 15-16, portions 102-108 are equivalent to a plurality of devices of the system since each portion can have separate bits] via the system interface and generate a first system identifier value as a function of the values of the identifications codes from the first plurality of devices [col. 3, lines 44-48, the IDCD code is generated which identifies the system 90 as a function of the identification codes 102-108].

Lulla does not explicitly disclose wherein the first plurality of devices is arranged and coupled in a scan chain, and the function used in generating the first system identifier value is further a function of respective positions of the first plurality of devices in a scan chain.

However, Geer discloses wherein the first plurality of devices is arranged and coupled in a scan chain, and the function used in generating the first system identifier value is further a function of respective positions of the first plurality of devices in a scan chain [col. 5, lines 29-35, the plurality of SRLs are arranged and coupled in a scan chain (fig. 1, SRLs 14 and 16). Retrieving the identification number is equivalent to generating the system identifier. The function of retrieving the identification number is a function of the locations of the SRLs in the scan chain, specifically “the chip ID or level ID SRLs indicating the location of the SRLs to retrieve the stored identification number.” The location of the SRLs is equivalent to the positions of the plurality of devices in a scan chain].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve upon the method of Lulla by implementing wherein the first plurality of devices is arranged and coupled in a scan chain, and the function used in generating the first system identifier value is further a function of respective positions of the first plurality of devices in a scan chain because it would provide Lulla with the enhanced capability of uniquely identifying integrated circuit chips adapted for use with scan design system and scan testing techniques [p. 2, paragraph 19-23].

Furthermore, taking claim 1 as exemplary, claim 20 is directed to similar limitations as claim 1 [see claim 1]. Therefore, claim 20 is rejected under the same rationale as claim 1, and in further view of Aralis.

**8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lulla, in view of Geer, in view of Aralis, and in further view of Dreyer et al (hereinafter Dreyer), U.S. Patent No. 5,794,066.**

**As per claim 3**, the modified Lulla does not explicitly disclose the method of claim 2, wherein the step of reading values from the first plurality of devices further comprises:

reading the value of a second register in each of the first plurality of devices, wherein each second register is user-programmable.

However, Dreyer discloses the use of reading the value of a second register [Dreyer, col. 6, lines 44-57, fig. 1, item 20] in each of the first plurality of devices, wherein each second register is user-programmable [Dreyer, col. 4, lines 56-61] for the purpose of providing an identification apparatus and for identifying a device during operation [col. 1, lines 66-67, col. 2, line 1].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve upon the method of the modified Lulla by implementing reading the value of a second register in each of the first plurality of devices, wherein each second register is user-programmable because it would provide the modified Lulla's method with the enhanced capability of providing an identification apparatus and for identifying a device during operation [col. 1, lines 66-67, col. 2, line 1].

**9. Claims 6, 7, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lulla, in view of Geer, in view of Aralis, and in further view of Jacobson et al (hereinafter Jacobson), U.S. Patent No. 5,841,867.**

**As per claim 6**, the modified Lulla does not explicitly disclose storing in the register of the at least one programmable logic device a checksum value derived from configuration data used in configuring the at least one programmable logic device.

However, Jacobson discloses the use of storing in the register [Jacobson, col. 7, lines 63-65, specifically the LFSR] of the at least one programmable logic device [Jacobson, col. 4, lines 24-25] a checksum value [Jacobson, col. 7, lines 24-25, specifically the signature] derived from configuration data used in configuring the at least one programmable logic device [Jacobson, col. 3, lines 45-49] for the purpose of verifying the PLD programming [Jacobson, col. 3, lines 22-24].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve upon the method of the modified Lulla by implementing storing in the register of the at least one programmable logic device a checksum value derived from configuration data used in configuring the at least one programmable logic device because it would provide the modified Lulla's method with the enhanced capability of verifying the programming of the PLD [Jacobson, col. 3, lines 22-24].

**As per claim 7**, the modified Lulla discloses wherein the generating step includes concatenating the values [Lulla, col. 5, line 6].

**As per claim 16**, Lulla discloses configuration states [Lulla, col. 3, lines 51-63, specifically CNFG and DEV indicate a state of the device. CNFG and DEV are inputs to the ID CODE GENERATION LOGIC which outputs the identification code, fig. 4]

The modified Lulla does not explicitly disclose generating checksum values from each of the configuration states.

However, Jacobson discloses the use of checksum values [Jacobson, col. 7, lines 24-25, specifically the signature] in order to verify programming PLDs [Jacobson, col. 3, lines 22-24].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve upon the method of the modified Lulla by implementing generating checksum values from each of the configuration states because it would provide the modified Lulla's method with the enhanced capability of verifying the programming of PLDs with respect to a sequence of input values [Jacobson, col. 8, lines 22-26].

**10. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lulla, in view of Geer, in view of Aralis, and in further view of Thiel et al (hereinafter Thiel), U.S. Patent No. 6,381,509 B1.**

**As per claim 18**, the modified Lulla does not explicitly disclose storing the generated system identifier.

However, Thiel discloses the use of storing the generated system identifier [col. 14, lines 65-67] for the purpose of generating and storing identifiers for parts and storing the identifiers by a data processing system [Abstract].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve upon the method of the modified Lulla by implementing storing the generated system identifier because it would provide the modified Lulla's method with the enhanced capability of generating and storing identifiers for parts and storing the identifiers by a data processing system [Abstract].

**11. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lulla, in view of Geer, in view of Aralis, and in further view of IBM Technical Disclosure Bulletin (hereinafter IBM), NA8909262.**

**As per claim 11**, the modified Lulla discloses inputting a control code to each of the first plurality of devices;

outputting the values of the identification codes serially from at least one of the first plurality of devices in response to the control code [Lulla, fig. 4, col. 3, lines 36-50].

The modified Lulla does not explicitly disclose outputting values of the identification codes from a boundary scan register.

However, IBM discloses the use of using a portion of the boundary scan register as the identification register [IBM, specifically "However, a portion of the boundary scan register can be used to implement the device identification function"] for the purpose of saving all the circuitry in the original identification register [IBM, p. 2, lines 4-7].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve upon the method of the modified Lulla by implementing outputting the values of the identification codes from a boundary-scan register because



Art Unit: 2181

it would provide the modified Lulla's method with the enhanced capability of saving all the circuitry in the original identification register [IBM, p. 2, lines 4-7].

**12. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lulla, in view of Geer, in view of Aralis, in view of IBM, and in further view of Jacobson.**

**As per claim 12**, the modified Lulla does not explicitly disclose wherein the control code is a boundary-scan SAMPLE instruction.

However, Jacobson discloses the use of the control code as a boundary-scan SAMPLE instruction [Jacobson, col. 2, lines 51-52] in order to select the boundary scan register [Jacobson, col. 2, lines 51-52].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve upon the method of the modified Lulla by implementing wherein the control code is a boundary-scan SAMPLE instruction because it would provide the modified Lulla's method with the enhanced capability of selecting the boundary scan register [Jacobson, col. 2, lines 51-52].

**As per claim 13**, the modified Lulla does not explicitly disclose wherein the control code is a boundary-scan EXTEST instruction.

Jacobson discloses the use of the control code as a boundary-scan EXTEST instruction [Jacobson, col. 2, lines 53-54] for the purpose of providing an efficient programming verification system for PLDs [col. 3, lines 22-24].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve upon the method of the modified Lulla by implementing

Art Unit: 2181

wherein the control code is a boundary-scan EXTEST instruction because it would provide the modified Lulla's method with the enhanced capability of providing an efficient programming verification system for PLDs [col. 3, lines 22-24].

**As per claim 14**, the modified Lulla does not explicitly disclose wherein the boundary scan register is one of an IDCODE register and a USERCODE register.

However, Lulla discloses a boundary-scan register, ID CODE register, and a USERCODE register [fig. 1] in between the TDI and TDO.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute one register for the other in order to achieve the predictable result of outputting values of identification codes from a register.

### ***Conclusion***

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

Art Unit: 2181

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FARLEY J. ABAD whose telephone number is (571) 270-3425. The examiner can normally be reached on Monday-Friday 7:30am-5:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/F. J. A./  
Examiner, Art Unit 2181

/Alford W. Kindred/  
Supervisory Patent Examiner, Art Unit 2181